REMARKS

Claims 1-25 remain in this application. Applicant respectfully requests reconsideration and review of the application in view of the following remarks.

Before addressing the merits of the rejections, Applicant provides the following brief description of the patent application. Generally, the patent application is directed to a switched mode power that comprises at least one power switch adapted to convey power between input and output terminals of the power supply, and a digital controller adapted to control operation of the power switches responsive to an output measurement of the power supply. More particularly, the digital controller comprises an analog-to-digital converter providing a digital error signal representing a voltage difference between the output measurement and a reference value, a digital filter providing a digital control output based on a sum of previous error signals and previous control outputs, an error controller adapted to modify operation of the digital filter upon an error condition, and a digital pulse width modulator providing a control signal to the power switch having a pulse width corresponding to the digital control output.

The analog-to-digital converter further comprises a windowed flash analog-to-digital converter having a transfer function defining a relationship between the voltage difference and corresponding digital values. The transfer function provides a substantially linear region at a center of a corresponding error window. In an embodiment of the invention, the transfer function of the analog-to-digital converter further comprises a first step size in the center of the error window and at least one other step size in a peripheral region of the error window that is larger than the first step size. The first step size and the other step sizes may each reflect a linear relationship between the voltage difference and the corresponding digital values. Alternatively, the first step size may reflect a linear relationship between the voltage difference and the corresponding digital values, and the other step sizes may each reflect a non-linear relationship between the voltage difference and the corresponding digital values.

The Examiner rejected Claims 1 and 17 under 35 U.S.C. § 103(a) as unpatentable over Stanley in combination with Melanson[1]. Applicant respectfully traverses this rejection.

Stanley discloses a pulse width modulator (PWM) audio power amplifier that includes a switch mode power converter. As shown in Fig. 2, PWM modulator 98 provides control signals through gate drivers 46 to control the operation of power switches in opposed current amplifier (OCA) 48. Output current and voltage sense signals from the OCA are returned through fast analog-to-digital converters (ADC) 96 that translate the sense signals to digital format. A digital signal processor (DSP) 18 further processes these digital signals to control the duty cycle provided by the PWM modulator in order to compensate for distortion. Stanley provides no further details of the ADC 96, and in particular, provides no detail of the transfer function implemented by the ADC 96.

Stanley further describes the desirability of providing linearity correction of the PWM audio amplifier, and the Examiner appears to misconstrue this linearity correction as corresponding to the use in the patent application of a linear region of the analog-to-digital transfer function (citing to Stanley at col. 10, line 30-50). Aside from the use of the similar term "linear," the patent application has nothing in common with the reference. In particular, Stanley provides output linearity by including a feed forward control path within the DSP (i.e., after the ADC 96). Stanley does not suggest or disclose altering the transfer function of the ADC 96. More pertinently, the patent application provides an analog-to-digital converter having a first step size in a center of a corresponding error window and a different (larger) step size in a peripheral region of the error window. Thus, the transfer function of the analog-to-digital converter actually provides a non-linear relationship between the voltage error signals and corresponding

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[1] The Office Action incorrectly identifies Melanson as U.S. Patent No. 5,079,498. In a telephone conference dated October 26, 2005, the Examiner advised the undersigned counsel that the correct patent number is U.S. Patent No. 6,373,334.

digital values. This is not suggested or disclosed by the reference.

The Examiner attempts to make up for the deficiency of Stanley by proposing the combination with Melanson. Melanson discloses a digital PWM amplifier that reduces distortion and noise by using a digital error signal to correct the feedback of a delta sigma modulator in real time. The analog-to-digital converter (ADC) 214 used to digitize the analog error signal includes dual integrator stages that provide a high conversion rate (see Fig. 3a). As with Stanley, Melanson does not suggest or disclose altering the transfer function of the ADC 96. In particular, Melanson does not suggest or disclose an analog-to-digital converter having a first step size in a center of a corresponding error window and a different (larger) step size in a peripheral region of the error window. Thus, the proposed combination of references fails to suggest or disclose all limitations of Claims 1 and 17, and this ground of rejection should be withdrawn.

The Examiner also rejected Claims 1-25 under 35 U.S.C. § 103(a) as unpatentable over Shimamori in combination with Cleasby et al. and further in combination with Chu et al. Applicant respectfully traverses this rejection.

Shimamori discloses a power conversion device having a digital control circuit for adjusting operation of the power conversion device in response to changing operating conditions. As shown in Fig. 4, a sensed signal (i.e., output voltage, output current, input voltage, temperature) of the power conversion device is digitized by A/D converter 35 and provided to processor 41. The processor 41 executes a control program to determine the duty cycle of the signal used to control the switch element of the power conversion device. Shimamori discloses that the control program comprises a digital filter, such as an infinite impulse response filter. The Examiner acknowledges that Shimamori does not disclose a digital pulse width modulator.

As with Stanley described above, Shimamori provides no details of the A/D converter 35. More specifically, Shimamori does not suggest or disclose an analog-to-digital converter having a first step size in a center of a corresponding error window and a different (larger) step size in a peripheral region of the error window. The proposed

combination with Cleasby et al. and Chu et al. fails to make up for this deficiency of Shimamori.

Cleasby discloses pulse width modulation for current control of a power conversion device. Cleasby fails to disclose a digital filter and also fails to disclose an analog-to-digital converter for digitizing the error signals. Moreover, Cleasby contains no teaching or suggestion that digital pulse width modulation could be adapted for use with a digital filter. Thus, there is no motivation whatsoever for the proposed combination of Cleasby with Shimamori.

Chu et al. discloses a method of tuning a proportional, integrating and derivative (PID) type control device. The parameters of the PID control device are managed such that the gain is restricted to a range between lower and upper limits. Chu contains no teaching or suggestion of an analog-to-digital converter having a first step size in a center of a corresponding error window and a different (larger) step size in a peripheral region of the error window. As with Cleasby, there is no motivation whatsoever for the proposed combination of Chu with the other references.

Accordingly, the Examiner has failed to present a *prima facie* case that any of the claims are obvious over the proposed combination of references. The foregoing grounds of rejection should therefore be withdrawn.

The Examiner also rejected Claims 1-25 under the judicially created doctrine of obviousness-type double patenting over U.S. Patent No. 6,850,046. Applicant encloses herewith a Terminal Disclaimer in compliance with 37 C.F.R. § 1.321(c), which is considered sufficient to obviate this ground of rejection.

In view of the foregoing, the Applicant respectfully submits that Claims 1-25 are in condition for allowance. Reconsideration and withdrawal of the rejections is respectfully requested, and a timely Notice of Allowability is solicited. To the extent it would be helpful to placing this application in condition for allowance, the Applicant encourages the Examiner to contact the undersigned counsel and conduct a telephonic interview.

To the extent necessary, Applicant petitions the Commissioner for a one-month extension of time, extending to October 29, 2005, the period for response to the Office Action dated June 29, 2005. A check in the amount of $250.00 is enclosed for the one-month extension of time ($120.00) pursuant to 37 CFR §1.17(a)(1) and $130.00 for the Terminal Disclaimer pursuant to 37 CFR § 1.20(d). The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0639.

Respectfully submitted,

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Brian M. Berliner
Attorney for Applicant
Registration No. 34,549

O'MELVENY & MYERS LLP
400 South Hope Street
Los Angeles, CA 90071-2899
Telephone: (213) 430-6000

Enclosure: Terminal Disclaimer